REMARKS

In response to the above-identified Office Action, Applicants amend the application and seek reconsideration thereof. In this response, Applicants do not amend, cancel, or add any claims. Accordingly, Claims 1-22 are pending.

I. Claims Rejected Under 35 U.S.C 103(a)

A. Claims 1-11, 13, 14, and 16-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent No. 5,150,312 issued to Beitel et al ("Beitel") in view of U.S. Patent No. 6,108,015 issued to Cross ("Cross"). Applicants respectfully traverse the rejection.

To establish a *prima facie* case of obviousness, the Examiner must show the cited references, combined, teach or suggest each of the elements of a claim. Claim 1 recites:

> "a display controller;
> an internal frame buffer coupled to the display controller; and
> a control circuitry to copy display data from an external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer."

Recognizing Beitel's failure to disclose a display controller and that buffer B is an internal frame buffer, the Examiner relies on Cross to supply the teaching. Cross discloses a display controller coupled to an internal frame buffer and an external frame buffer, from either of which display data is retrieved to refresh the display (FIG. 1). Applicants submit that a frame buffer is the final storage area for an image shown by a display. Thus, a display controller retrieves display data directly from a frame buffer to refresh the display. Beitel's buffer B is not a final storage area of display data. Buffer B at most is a temporary storage area for superimposing an animated object onto a portion of an image. The content of buffer B is not directly sent to the display; rather, it is forwarded to a frame buffer (display memory 1) to form display data therein for display (block 26 of FIG. 3). Assuming for the sake of argument that Beitel's system is modified by the display controller of Cross, the display controller would not be able to retrieve display data directly from buffer B. Buffer B merely holds the portion of an image containing an animated object and its

adjacent area (FIG. 2). The animated object may appear anywhere in the entire image frame, thus requiring a final integration to be performed at display memory 1 with the rest of the image portion to form display data. Without the final integration at display memory 1, a display controller would not know how to properly refresh the display given the image portion stored in buffer B. As buffer B is not the final storage area for display data and does not hold the display data readily for display, buffer B cannot possibly teach or suggest the frame buffer as claimed.

Moreover, a skilled person in the art would at most apply Cross's teaching to modify Beitel's display memory 1 to include both an internal and an external frame buffer, because the display memory is the final storage area for holding the display data. However, the modified system would not "copy display data from the external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer" as recited in Claim 1. There is no teaching or suggestion in either Beitel or Cross of copying display data from one frame buffer to another frame buffer. Thus, Beitel in view of Cross does not teach or suggest each of the elements of Claim 1.

With regard to Claim 9, Applicants have defined in the Specification that "internal/external memory array" and "internal/external frame buffer" are used interchangeably (paragraph 10 of Specification). Thus, analogous discussion applies to independent Claims 9 and 16.

Claims 2-8, 10, 11, 13, 14, and 17-22 respectively depend from Claims 1, 9, and 16 and incorporate the limitations thereof. Thus, for at least the foregoing reasons, Beitel in view of Cross does not anticipate these dependent claims.

Moreover, Claim 2 recites "the display data is copied into the internal frame buffer simultaneously with the display controller reading the display data from the external frame buffer." (Emphasis added). The Examiner asserts that the display data is copied into buffer B simultaneously with the CPU containing the display controller reading the display data from display memory 1. However, the cited passage "the first image disappears from the present portion of the second image while simultaneously appearing within the next portion of the second image, thereby avoiding display screen flicker" (col. 1, lines 63-68) does not support this assertion. The

avoidance of screen flicker is achieved, as explained by Beitel at col. 4, lines 26-31, by "writing the buffer B image to the screen memory 1" to cause "the object to be totally erased from the region 10a while simultaneously being written to the region 10b." As buffer B contains both 10a (where the object is erase) and 10b (where the object is written), this cited passage at most suggests copying from buffer B to screen memory 1. According to FIG. 3 of Beitel, the copying (or transferring) operation is performed before, not simultaneously with, the display data being read from display memory 1 for display at the end of block 26. Nothing in Beitel indicates that copying display data into buffer B occurs simultaneously with reading the display data from display (screen) memory 1. Thus, Claim 2 is not obvious over Beitel in view of Cross for this additional reason.

Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 1-11, 13, 14, and 16-22 are requested.

B. Claims 9-12 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Beitel in view of U.S. Pre-Grant Patent Application No. 2004/10150647A1 applied for by Aleksic et al. ("Aleksic").

The Examiner relies on Aleksic for disclosing a graphics chip containing a display controller, an internal memory array, and control circuitry. However, Aleksic does not cure the defect of Beitel for failing to teach the internal/external frame buffers (i.e., the internal/external memory arrays) as claimed. Beitel discloses that buffer B is located in main memory 4 (col. 2, line 41), which cannot possibly be placed on the limited space of a graphic chip. Moreover, assuming for the sake of argument that a skilled person may modify Beitel to place buffer B on a graphics chip, buffer B is not a frame buffer for the reasons mentioned above with regard to Claim 1. Thus, Beitel in view of Aleksic does not teach or suggest each of the elements of Claim 9 and its dependent Claims 10-12 and 15. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 9-12, and 15 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-22 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Erin Flynn — 11-16-05 (Date)